

## **BatterySwitch™**

### **General Description**

Analogic Tech™'s AAT7204 is a dual 2.5V rated N channel MOSFET designed for use in battery packs, cellular phones and battery powered portable equipment. Utilizing Analogic Tech's proprietary ultra high density TrenchDMOS™ process, the AAT7204 achieves performance normally found in products that are rated to block only 20V in one that blocks 25V. Featuring a small footprint and low profile of <1.2mm, the TSSOP8 package is ideal for use in battery and load management applications where height and size are critical.

## **TSSOP8 Package**

 $V_{DS(MAX)} = 25V$ 

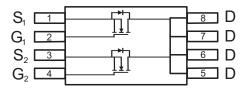
 $I_{D(MAX)} = 6.0A^{1} \otimes 25^{\circ}C$ Low  $R_{DS(ON)}$ :

 $26 \text{ m}\Omega @V_{GS} = 4.5V$ 

 $40 \text{ m}\Omega @V_{GS} = 2.5V$ 

Optimized for battery protection

**Features** 



## **Applications**

- Li Ion Battery Packs
- Cellular and Cordless Telephones
- Battery-powered portable equipment

## **Absolute Maximum Ratings** (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Description		10 sec	DC	Units	
V <sub>DS</sub>	Drain-Source Voltage		25		V	
$V_{GS}$	Gate-Source Voltage		±12			
I <sub>D</sub>	Continuous Drain Current @ T <sub>J</sub> =150°C ¹	$T_A = 25^{\circ}C$	6.0	5.1		
		T <sub>A</sub> = 70°C	4.8	4.1		
I <sub>DM</sub>	Pulsed Drain Current (10µs pulse width)		±30		Α	
I <sub>S</sub>	Continuous Source Current (Source-Drain Diode) 1		1.7	1.3		
I <sub>SM</sub>	Pulsed Source Current (Source-Drain Diode) 3		±30			
P <sub>D</sub>	Maximum Power Dissipation <sup>1</sup>	T <sub>A</sub> = 25°C	1.5	1.1	W	
		T <sub>A</sub> = 70°C	1.0	0.7		
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range		-55 to 150		°C	

## **Thermal Characteristics**

Symbol	Description	Value	Units
$R_{\theta JA}$	Typical Junction-to-Ambient <sup>2</sup>	88	°C/W
$R_{\theta JA2}$	Maximum Junction-to-Ambient, one MOSFET on, t <10s 1		°C/W
$R_{\theta JF}$	Typical Junction-to-Foot 1	40	°C/W



# **Electrical Characteristics** (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Description	Conditions	Min	Тур	Max	Units	
DC Charac	DC Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	25			V	
	Drain-Source ON-Resistance <sup>3</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.0A		21	26	mΩ	
$R_{DS(ON)}$		V <sub>GS</sub> =2.5V, I <sub>D</sub> =4.8A		32	40	11122	
$I_{D(ON)}$	On-State Drain Current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V (10μs pulse width)	30			Α	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_{D}=250\mu A$	0.6			V	
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±100	nA	
1	Drain Source Leakage Current	$V_{GS}$ =0V, $V_{DS}$ =25V			1		
I <sub>DSS</sub>		$V_{GS}$ =0V, $V_{DS}$ =20V, $T_J$ =70°C <sup>4</sup>	5		- μΑ		
9 <sub>fs</sub>	Forward Transconductance 3	$V_{DS}$ =5V, $I_{D}$ =6.0A		19		S	
Dynamic C	Dynamic Characteristics ⁴						
$Q_G$	Total Gate Charge	$V_{DS}$ =15V, $R_{D}$ =3.0 $\Omega$ , $V_{GS}$ =4.5V		16	23		
$Q_{GS}$	Gate-Source Charge	$V_{DS}$ =15V, $R_{D}$ =3.0 $\Omega$ , $V_{GS}$ =4.5V		2.7		nC	
$Q_{GD}$	Gate-Drain Charge	$V_{DS}$ =15V, $R_{D}$ =3.0 $\Omega$ , $V_{GS}$ =4.5V		3.2			
t <sub>D(ON)</sub>	Turn-ON Delay	$V_{DD}$ =15V, $V_{GS}$ =4.5V, $R_{D}$ =3.0 $\Omega$ , $R_{G}$ =6 $\Omega$		10			
t <sub>R</sub>	Turn-ON Rise Time	$V_{DD}$ =15V, $V_{GS}$ =4.5V, $R_{D}$ =3.0 $\Omega$ , $R_{G}$ =6 $\Omega$		14		ns	
t <sub>D(OFF)</sub>	Turn-OFF Delay	$V_{DD}$ =15V, $V_{GS}$ =4.5V, $R_{D}$ =3.0 $\Omega$ , $R_{G}$ =6 $\Omega$		31		115	
t <sub>F</sub>	Turn-OFF Fall Time	$V_{DD}$ =15V, $V_{GS}$ =4.5V, $R_{D}$ =3.0 $\Omega$ , $R_{G}$ =6 $\Omega$		17			
Source-Drain Diode Characteristics							
$V_{SD}$	Source-Drain Forward Voltage <sup>3</sup>	V <sub>GS</sub> =0, I <sub>S</sub> =6.0A			1.2	V	
I <sub>S</sub>	Continuous Diode Current <sup>1</sup>				1.7	Α	

Note 1: Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 10 second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in many applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta FA}$  is determined by PCB design. Actual maximum continuous current is limited by the application's design.

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Note 2: Steady state thermal response while mounted on a 1" x 1" PCB with maximum copper area is provided for comparison with other devices. This test condition approximates many battery pack applications.

Note 3: Pulsed measurement 300 µs, single pulse.

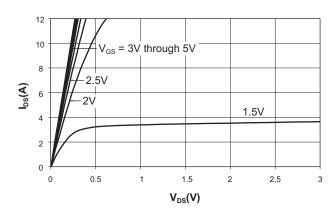
Note 4: Guaranteed by design. Not subject to production testing.



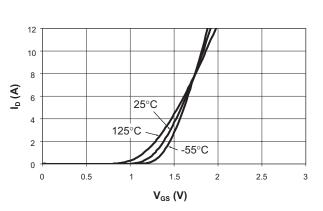
## **Typical Characteristics**

(T<sub>J</sub> = 25°C unless otherwise noted)

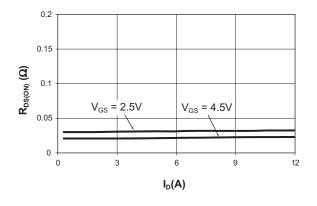
#### **Output Characteristics**



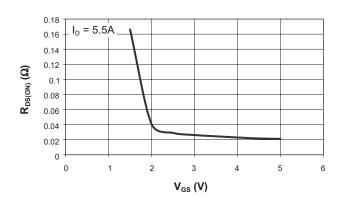
#### **Transfer Characteristics**



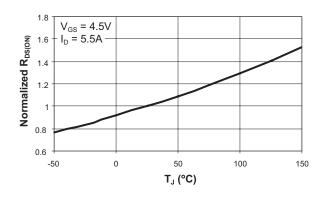
**On-Resistance vs. Drain Current** 



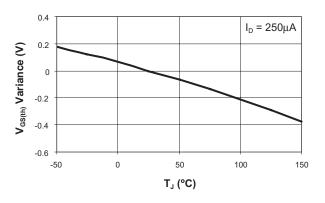
On-Resistance vs. Gate to Source Voltage



**On-Resistance vs Junction Temperature** 



Threshold Voltage

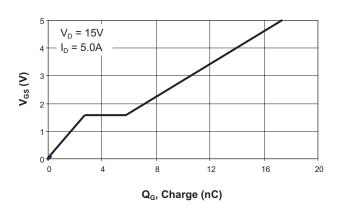




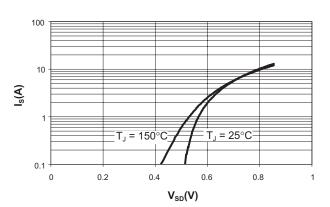
# **Typical Characteristics**

 $T_J = 25^{\circ}$ C unless otherwise noted)

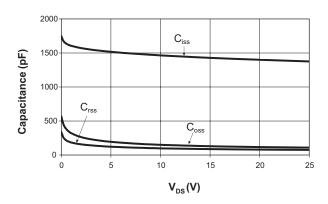
### **Gate Charge**



### Source-Drain Diode Forward Voltage



### Capacitance





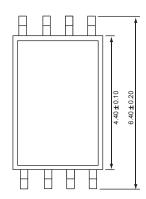
# **Ordering Information**

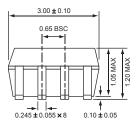
Package	Marking	Part Number (Tape and Reel)
TSSOP-8	7204	AAT7204IHS-T1

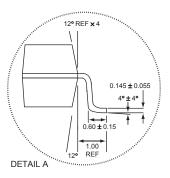
Note: Sample stock is generally held on all part numbers listed in **BOLD**.

# **Package Information**

TSSOP-8







All dimensions in millimeters.



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